WHAT IS CLAIMED IS:

1. A information handling system comprising:

a processor having a THERMTRIP output;

a power supply coupled to the processor for operating the processor; and

a thermal trip power control circuit comprising:

a latch having a CLK input coupled to the THERMTRIP output of the processor and CLR input coupled to a user-activated control; and

a gate having an input coupled to the output of the latch and an output coupled to a PS_{ON} input of the power supply.

2. The information handling system as defined in Claim 1, further comprising:

signal conditioning means coupled between the THERMTRIP output of the processor and the CLK input of the latch for conditioning a processor THERMTRIP signal so that an overheating condition of the processor causes a transition at the CLK input of the latch.

3. The information handling system as defined in Claim 2, wherein the signal conditioning means comprises:

a level shifter having an input coupled to the THERMTRIP output of the processor; and

an inverter coupled to an output of the level shifter.

4. The information handling system as defined in Claim 3, wherein the signal conditioning means is operable to cause a negative-going transition in the THERMTRIP signal to result in a positive-going transition at the CLK input of the latch.

5. The information handling system as defined in Claim 4, further comprising:

an isolation switch coupled between the signal conditioning means and the CLK input of the latch, the isolation switch operable to selectively couple the THERMTRIP signal to the CLK input of the latch.

6. The information handling system as defined in Claim 5, wherein the isolation switch is operable to couple THERMTRIP signal to the CLK input of the latch when a PS

signal is asserted and to isolate the THERMTRIP signal from the CLK input of the latch when the PS_G signal CLK is not asserted.

7. The information handling system as defined in Claim 6, wherein the isolation switch has an input node coupled to the signal conditioning means, an output node coupled to the CLK input of the latch, and a control node coupled to the PS_G signal.

8. The information handling system as defined in Claim 7, wherein the isolation switch comprises an FET.

9. The information handling system as defined in Claim 1, further comprising:

an isolation switch coupled between the THERMTRIP output of the processor and the CLK input of the latch, the isolation circuit operable to selectively couple the THERMTRIP signal to the CLK input of the latch in response to the PS_G signal.

10. The information handling system as defined in Claim 9, further comprising a signal conditioner that comprises:

a level shifter having an input coupled to the THERMTRIP output of the processor; and

an output of the level shifter and an output coupled to the isolation circuit.

11. The information handling system as defined in Claim 10, wherein the signal conditioner is operable to cause a negative-going transition in the THERMTRIP signal to result in a positive-going transition in the THERMTRIP signal at the isolation circuit.

12. The information handling system as defined in Claim 10, wherein the isolation switch is operable to couple THERMTRIP signal to the CLK input of the latch when a PS signal is asserted and to isolate the THERMTRIP signal from the CLK input of the latch when the PS_G signal CLK is not asserted.

13. The information handling system as defined in Claim 12, wherein the isolation switch has an input node coupled to the signal conditioning means, an output node coupled to the CLK input of the latch, and a control node coupled to the PS_G signal.

14. The information handling system as defined in Claim 1, wherein the CLK input of the latch is coupled to the processor.

15. The information handling system as defined in Claim 14, wherein the CLK input of the latch is coupled to the processor through an isolation circuit.

16. The information handling system as defined in Claim 15, wherein the isolation circuit operates to prevent the latch from changing state until the power supply is demonstrated to be properly operating.

17. The information handling system as defined in Claim 16, wherein the isolation circuit comprises a semiconductor switching device having an input node coupled to the processor, and output node coupled to the CLK input of the latch and a control node coupled to the power supply.

18. In an information handling system comprising a processor and a power supply, a method of controlling the power supply in response to an overheating condition of the processor, the method comprising:

receiving a THERMTRIP signal from the processor, the THERMTRIP signal indicative of a processor overheating condition;

coupling the THERMTRIP signal to a latch circuit so that the latch circuit provides at an output a THERMTRIP_PS_{DIS} signal to the power supply so as to disable the power supply.

19. The method as defined in Claim 18, wherein the THERMTRIP signal is coupled to the latch circuit through an isolation switch so that invalid signals are isolated from the latch circuit.

20. The method as defined in Claim 19, wherein the isolation switch has an input node coupled to the THERMTRIP signal, and output node coupled to the latch, and a control node coupled to a PS_G signal.

21. The method as defined in Claim 20, wherein the isolation circuit comprises a FET.

22. The method as defined in Claim 18, wherein the THERMTRIP signal is coupled to the latch circuit through a signal conditioner.

23. The method as defined in Claim 22, wherein the signal conditioner comprises:

a level shifter having an input coupled to the THERMTRIP output of the processor; and

an inverter coupled to the output of the level shifter.

24. The method as defined in Claim 23, wherein the signal conditioner is operable to cause a negative-going transition in the THERMTRIP signal to result in a positive-going transition at a CLK input of the latch.

25. The method as defined in Claim 24, further comprising:

an isolation switch coupled between the signal conditioner and the CLK input of the latch, the isolation switch operable to selectively couple the THERMTRIP signal to the CLK input of the latch.

26. The method as defined in Claim 25, wherein the isolation switch is operable to couple THERMTRIP signal to the CLK input of the latch when a PS_G signal is asserted and to isolate the THERMTRIP signal from the CLK input of the latch when the PS_G signal CLK is not asserted.

27. The method as defined in Claim 26, wherein the isolation switch has an input node coupled to the signal conditioner, an output node coupled to the CLK input of the latch, and a control node coupled to the PS_G signal.

28. The method as defined in Claim 18, wherein a transition in the received THERMTRIP signal causes a transition in a CLK input of the latch so that the latch provides a THERMTRIP_PS_{DIS} signal to the power supply so as to disable the power supply.

29. The method as defined in Claim 18, further comprising:
coupling a user-activated signal to a CLR input of the latch so as to CLR the THERMTRIP_PS_{DIS} signal and thereby enable the power supply.

30. The method as defined in Claim 29, wherein the user-activated signal is a PS_{ON} signal from a information handling system PWR button.

31. The method as defined in Claim 18, wherein the THERMTRIP_PS_{DIS} is coupled to a first input of a logic circuit, the logic circuit having an output coupled to the PS_{ON} input of the power supply so that the power supply is disabled whenever the THERMTRIP_PS_{DIS} signal is asserted.

32. The method as defined in Claim 32, further comprising:
coupling a PS_{DIS} signal to a second input of the logic circuit so that the power supply is disabled whenever the PS_{DIS} signal is asserted.

33. A thermal trip power control circuit comprising:
a latch having a CLK input coupled to a THERMTRIP output of a processor and CLR input coupled to a user-activated control; and
a gate having an input coupled to the output of the latch and an output coupled to a PS_{ON} input of a power supply.

34. The thermal trip power control circuit as defined in Claim 33, further comprising:
signal conditioning means coupled between the THERMTRIP output and the CLK input of the latch for conditioning a processor THERMTRIP signal so that an overheating condition of the processor causes a transition at the CLK input of the latch.

35. The thermal trip power control circuit as defined in Claim 34, wherein the signal conditioning means comprises:
a level shifter having an input coupled to the THERMTRIP output; and
an inverter coupled to an output of the level shifter.

36. The thermal trip power control circuit as defined in Claim 35, wherein the signal conditioning means is operable to cause a negative-going transition in the THERMTRIP signal to result in a positive-going transition at the CLK input of the latch.

37. The thermal trip power control circuit as defined in Claim 36, further comprising:

an isolation switch coupled between the signal conditioning means and the CLK input of the latch, the isolation switch operable to selectively couple the THERMTRIP signal to the CLK input of the latch.

38. The thermal trip power control circuit as defined in Claim 37, wherein the isolation switch is operable to couple THERMTRIP signal to the CLK input of the latch when a PS signal is asserted and to isolate the THERMTRIP signal from the CLK input of the latch when the PS_G signal CLK is not asserted.

39. The thermal trip power control circuit as defined in Claim 38, wherein the isolation switch has an input node coupled to the signal conditioning means, an output node coupled to the CLK input of the latch, and a control node coupled to the PS_G signal.

40. The thermal trip power control circuit as defined in Claim 39, wherein the isolation switch comprises an FET.

41. The thermal trip power control circuit as defined in Claim 33, further comprising:

an isolation switch coupled between the THERMTRIP output of the processor and the CLK input of the latch, the isolation circuit operable to selectively couple the THERMTRIP signal to the CLK input of the latch in response to the PS_G signal.

42. The thermal trip power control circuit as defined in Claim 41, further comprising a signal conditioner that comprises:

a level shifter having an input coupled to the THERMTRIP output of the processor; and

an output of the level shifter and an output coupled to the isolation circuit.

43. The thermal trip power control circuit as defined in Claim 42, wherein the signal conditioner is operable to cause a negative-going transition in the THERMTRIP signal to result in a positive-going transition in the THERMTRIP signal at the isolation circuit.

44. The thermal trip power control circuit as defined in Claim 42, wherein the isolation switch is operable to couple THERMTRIP signal to the CLK input of the latch when a PS signal is asserted and to isolate the THERMTRIP signal from the CLK input of the latch when the PS_G signal CLK is not asserted.

45. The thermal trip power control circuit as defined in Claim 44, wherein the isolation switch has an input node coupled to the signal conditioning means, an output node coupled to the CLK input of the latch, and a control node coupled to the PS_G signal.

46. The thermal trip power control circuit as defined in Claim 33, wherein the CLK input of the latch is coupled to the processor.

47. The thermal trip power control circuit as defined in Claim 46, wherein the CLK input of the latch is coupled to the processor through an isolation circuit.

48. The thermal trip power control circuit as defined in Claim 47, wherein the isolation circuit operates to prevent the latch from changing state until the power supply is demonstrated to be properly operating.

49. The thermal trip power control circuit as defined in Claim 48, wherein the isolation circuit comprises a semiconductor switching device having an input node coupled to the processor, and output node coupled to the CLK input of the latch and a control node coupled to the power supply.